MAEDA et al.
Serial No. 10/714,935
Response to Office Action dated July 7, 2006

AMENDMENTS TO THE SPECIFICATION:

Please replace the paragraph beginning at page 1, line 4 with the following amended paragraph:

This Nonprovisional application claims priority under 35 U.S.C. § 119(a) of ~~on~~ Patent Application No. 2002/340044 filed in Japan on November 22, 2002, the entire contents of which are hereby incorporated by reference.

Please replace the paragraph beginning on page 6, line 7 with the following amended paragraph:

Some of the data signal line driving circuits include ~~includes~~ a plurality of shift registers, each of which has a less number of output stages, i.e., a less number of flip-flops F/F. In the present specification, a shift register block refers to a group of shift registers including a required number of output stages regardless of the number of systems of shift register.

Please replace the paragraph beginning on page 7, line 4 with the following amended paragraph:

Further, a plurality of waveform processing circuits ~~circuit~~ WR1(1) through WR1(m), which are respectively supplied with outputs of the flip-flops F/F1(1) through F/F1(m) constituting the first system shift register sr1, are provided between the first system shift register sr1 and the second system shift register sr2. Likewise, a plurality of waveform processing circuit WR2(1) through WR2(m), which are respectively supplied with outputs of the flip-flops F/F2(1) through F/F2(m) constituting the second system shift register sr2, are provided in parallel with the second system shift register sr2.

Please replace the paragraph beginning on page 26, line 17 with the following amended paragraph:

One notable feature of the foregoing circuit block is positioning of the plurality of waveform processing circuits WR (1) through WR (n) which are respectively supplied with output signals of the plurality of flip-flops of the shift register SR. As shown in Figure 1, the waveform processing circuits WR (1) through WR (n) are respectively provided between each adjacent pair ~~pairs~~ of the plurality of flip-flops F/F (1) through F/F (n) which are connected in a form of cascade connection for constituting the shift register SR.

Please replace the paragraph beginning on page 34, line 19 with the following amended paragraph:

The first shift register SR1 is constituted of a plurality of flip-flops F/F1(1), F/F1(2), ... F/F1(m), which are supplied with a clock signal SCK1 and a start pulse signal SSP1 as control signals. The second shift register SR2 is constituted of a plurality of flip-flops F/F2(1), F/F2(2), ... F/F2(m), which are supplied with a clock signal SCK2 and a start pulse signal SSP2 as control signals. The first ~~fist~~ system shift register SR1 and the second system shift register SR2 are adjacently disposed in the vertical direction. In this point, this example is the same as that of Figure 18 having a conventional two-system shift registers sr1 and sr2.